

**REMARKS**

Claims 1-13 and 18-27 are now pending. Claims 14-17 have been canceled. Claims 18-27 have been withdrawn. Claims 1 and 4 have been amended.

**Election/Restrictions**

The Patent Office stated a restriction to one of the following inventions under 35 U.S.C. §121:

- I. Claims 1-17
- II. Claims 18-22
- III. Claims 23-27

Applicant elects group I, claims 1-17, with traverse.

**35 U.S.C. § 102(b)**

The Patent Office rejected Claims 1-4, 7, 11-17 under 35 U.S.C. 102(b) as being anticipated by Jin et. al., U.S. Patent No. 6,351,039 (Jin).

Applicant respectfully traverses. Applicant respectfully submits claim 1 includes elements that have not been disclosed by Jin. Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration. *W.L. Gore & Assocs. v. Garlock*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984). Further, “anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim.” *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)). Emphasis added.

For example, claim 1 recites a plurality of conductive plugs electrically interconnecting the single gate electrode and the gate signal line. This is advantageous as it increases a number of contacts and removes extraneous polysilicon routing whereby the gate resistance is reduced. (Instant Application, Page 3, Paragraph [0007]).

Jin fails to teach, disclose or suggest a plurality of conductive plugs electrically interconnecting the single gate electrode and the gate signal line. Rather, Jin teaches a system whereby each plug is coupled to an individual gate electrode. The Patent Office points to FIGS. 3a and 3b of Jin for the rejection of claim 1. However, FIGS. 3a and 3b depict multiple conductive plugs electrically coupled to multiple gate electrodes. Consequently, Jin fails to teach, disclose, or suggest an element of claim 1. Under *Lindemann*, a *prima facie* case of anticipation has not been established for claim 1. Thus, claim 1 is believed allowable. Claims 2-4, 7 and 11-13 are believed allowable due to their dependence upon claim 1.

**35 U.S.C. § 103(a)**

The Patent Office rejected Claims 5-6 and 8-10 under 35 U.S.C. 103(a) as being unpatentable over Jin et. al., U.S. Patent No. 6,351,039 (Jin).

Applicant respectfully traverses. It is contended that claims 5-6 and 8-10 under this section depends on independent claim 1 which is non-anticipatory and non-obvious based on the rationale above. Thus, claims 5-6 and 8-10 (which depends on independent claim 1) should be allowed.

**CONCLUSION**

In light of the forgoing amendments and arguments, reconsideration of the claims is hereby requested, and a Notice of Allowance is earnestly solicited.

Respectfully submitted,  
LSI Logic, Inc.

A handwritten signature in black ink, reading "Chad W. Swantz", written over a horizontal line.

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